

PATENT
P57002**IN THE CLAIMS**

Please amend claims 1, 8, 14 and 21 as follows:

1 1. (Currently Amended) A thin film transistor, comprising a source electrode, a
2 drain electrode, a gate electrode and a semiconductor layer, wherein one of the source
3 electrode, the drain electrode, and the gate electrode comprises an aluminum alloy layer
4 disposed between a pair of titanium layers, [[and]] wherein a diffusion prevention layer is
5 interposed between the aluminum alloy layer and each of the pair of titanium layers, and
6 wherein the aluminum alloy layer comprises at least one selected from a group consisting
7 of silicon, copper, neodymium, platinum and nickel.

1 2. (Original) The thin film transistor of claim 1, wherein the aluminum alloy layer
2 comprises about 0.1 to 5 wt% of at least one element selected from a group consisting of
3 silicon, copper, neodymium, platinum and nickel.

Claim 3. (Canceled)

1 4. (Previously Presented) The thin film transistor of claim 1, wherein each
2 diffusion prevention layer is made of titanium nitride.

1 5. (Previously Presented) The thin film transistor of claim 4, wherein each
2 titanium nitride layer has a thickness between 100 and 500Å.

PATENT
P57002

1 6. (Previously Presented) The thin film transistor of claim 4, wherein each
2 titanium nitride layer contains 5 to 85 wt% of nitrogen.

1 7. (Original) The thin film transistor of claim 1, each electrode being absent of
2 pure aluminum.

1 8. (Currently Amended) A flat panel display, comprising:
2 a substrate;
3 a first plurality of thin film transistors formed on a surface of the substrate, the
4 first plurality of thin film transistors comprising first source electrodes, first drain
5 electrodes, first gate electrodes, and semiconductor layers;
6 a plurality of first conductive lines electrically connected to the first source
7 electrodes; and
8 a plurality of second conductive lines electrically connected to the first gate
9 electrodes;
10 a second plurality of thin film transistors, wherein the first drain electrodes of the
11 first plurality of thin film transistors are electrically connected to gate electrodes of the
12 second plurality of thin film transistors, wherein one of the first source electrodes, the
13 first drain electrodes, the first gate electrodes, the plurality of first conductive lines, and
14 the plurality of second conductive lines comprises an aluminum alloy layer and a titanium
15 layer formed on both surfaces of the aluminum alloy layer, [[and]] wherein a diffusion

PATENT
P57002

16 prevention layer is interposed between the aluminum alloy layer and the titanium layers.
17 and wherein the aluminum alloy layer comprises at least one selected from a group
18 consisting of silicon, copper, neodymium, platinum and nickel.

1 9. (Original) The flat panel display of claim 8, wherein the aluminum alloy layer
2 comprises about 0.1 to 5 wt% of at least one element selected from the group consisting
3 of silicon, copper, neodymium, platinum and nickel.

Claim 10. (Canceled)

1 11. (Previously Presented) The flat panel display of claim 8, wherein each
2 diffusion prevention layer is made of titanium nitride.

1 12. (Previously Presented) The flat panel display of claim 11, wherein each
2 titanium nitride layer has a thickness between 100 to 500Å.

1 13. (Original) The flat panel display of claim 11, wherein each titanium nitride
2 layer contains 5 to 85 wt% of nitrogen.

1 14. (Currently Amended) A TFT, comprising:
2 a source electrode, a gate electrode and a drain electrode; and

PATENT
P57002

3 a semiconductor layer between the source electrode and the drain electrode,
4 wherein one of said source electrode and said drain electrode contain an aluminum alloy
5 layer bounded by a pair of titanium layers and not a pure aluminum layer, [[and]] wherein
6 said source electrode and said drain electrode each comprising a TiN diffusion prevention
7 layer between the aluminum alloy layer and each titanium layer, and wherein the
8 aluminum alloy layer comprises at least one selected from a group consisting of silicon,
9 copper, neodymium, platinum and nickel.

1 15. (Original) The TFT of claim 14, wherein the aluminum alloy layer comprises
2 about 0.1 to 5 wt% of at least one element selected from the group consisting of silicon,
3 copper, neodymium, platinum and nickel.

Claim 16. (Canceled)

1 17. (Original) The TFT of claim 14, said semiconductor layer being absent of
2 aluminum after said TFT is subjected to a heat treatment of at least 300 degrees Celsius.

1 18. (Original) The TFT of claim 14, said semiconductor layer being primarily
2 made of silicon and said semiconductive layer forming a conductive channel between said
3 source electrode and said drain electrode upon application of a voltage to the gate
4 electrode after said TFT is exposed to heat of at least 300 degrees Celsius.

PATENT
P57002

1 19. (Original) The TFT of claim 14, said source electrode and said drain electrode
2 both being formed of aluminum alloy and both being absent pure aluminum.

Claim 20. (Canceled)

1 21. (Currently Amended) A process for making a flat panel display, comprising:
2 forming a first plurality of thin film transistors formed on a surface of a substrate,
3 the first plurality of thin film transistors comprising first source electrodes, first drain
4 electrodes, first gate electrodes, and semiconductor layers;
5 electrically connecting a plurality of first conductive lines to the first source
6 electrodes;
7 electrically connecting a plurality of second conductive lines to the first gate
8 electrodes; and
9 forming a second plurality of thin film transistors, electrically connecting the first
10 drain electrodes of the first plurality of thin film transistors to gate electrodes of the
11 second plurality of thin film transistors, wherein one of the first source electrodes, the
12 first drain electrodes, the first gate electrodes, the plurality of first conductive lines, and
13 the plurality of second conductive lines comprises an aluminum alloy layer and a titanium
14 layer formed on both surfaces of the aluminum alloy layer, and interposing a diffusion
15 prevention layer between the aluminum alloy layer and the titanium layers, and wherein
16 the aluminum alloy layer comprises at least one selected from a group consisting of
17 silicon, copper, neodymium, platinum and nickel.

PATENT
P57002

1 22. (Previously Presented) The process of claim 21, comprised of making the
2 aluminum alloy layer from an aluminum alloy comprising about 0.1 to 5 wt% of at least
3 one element selected from the group consisting of silicon, copper, neodymium, platinum
4 and nickel.

1 23. (Previously Presented) The process of claim 21, comprised of making the
2 diffusion prevention layers of titanium nitride.

1 24. (Previously Presented) The process of claim 23, comprised of making the
2 titanium nitride layers with a thickness between 100 to 500Å.